What is claimed is:

1. A method of controlling a bias voltage of a Mach-Zender modulator (MZM) performing a non-return-to-zero (NRZ) modulation of an optical signal, comprising:

generating a digital pilot signal;

modulating the MZM using the digital pilot signal;

coupling a portion of an optical output signal from the MZM to a light detector;

processing an output signal of the light detector using a digital correlation filter to recover the digital pilot signal; and

demodulating the recovered digital pilot signal to produce a feedback signal controlling the bias voltage of the MZM.

2. The method of claim 1 wherein the digital pilot signal is a digitized sinusoidal signal.

3. The method of claim 1 wherein the processing step further comprises:

filtering the output signal of the light detector using a band-path filter;

digitizing the output signal of the light detector using an analog-to-digital converter;

sampling the output signal of the analog-to-digital converter; and

applying a digital correlating technique recover at least one of the digital pilot signal or a first harmonic of the digital pilot signal.

4. The method of claim 3 wherein the digital correlating technique further comprises:

time-domain averaging of a pre-determined number of samples of the output signal of the analog-to-digital converter.

5. The method of claim 1 wherein the demodulating step further comprises:

using a digital synchronous demodulating technique, and

generating a signal maintaining a bias voltage of the MZM at a quadrature bias point.

6. A method of controlling bias voltages of an input Mach-Zender modulator (MZM)

and an output MZM coupled for performing a return-to-zero (RZ) modulation or a carrier suppressed RZ (CSRZ) modulation of an optical signal, comprising:

generating a digital pilot signal;

modulating sequentially the input MZM or the output MZM using the digital pilot signal;

coupling a portion of an optical output signal from the output MZM to a light detector;

processing an output signal of the light detector using a digital correlation filter to recover the digital pilot signal; and

demodulating the detected digital pilot signal to produce a feedback signal controlling a bias voltage of an MZM modulated using the digital pilot signal during at least a data sampling period of the processing step.

7. The method of claim 6 wherein the digital pilot signal is a digitized sinusoidal signal.

8. The method of claim 6 wherein the processing step further comprises:

filtering the output signal of the light detector using a band-path filter;

digitizing the output signal of the light detector using an analog-to-digital converter;

sampling the output signal of the analog-to-digital converter; and

applying a digital correlating technique recover at least one of the digital pilot signal or a first harmonic of the digital pilot signal.

9. The method of claim 8 wherein the digital correlating technique further comprises:

time-domain averaging of a pre-determined number of samples of the output signal of the analog-to-digital converter.

10. The method of claim 6 wherein the demodulating step further comprises:

using a digital synchronous demodulating technique, and

generating a signal maintaining a bias voltage of the MZM at a quadrature bias point.

11. An apparatus for controlling a bias voltage of a Mach-Zender modulator (MZM) performing a non-return-to-zero (NRZ) modulation of an optical signal, comprising:

a generator of a digital pilot signal modulating the MZM;

a bias circuit generating a bias voltage for the MZM;

a light detector of a portion of an optical output signal from the MZM; and

a digital signal processor processing an output signal of the light detector, the processor coupled to a control input of the bias circuit.

12. The apparatus of claim 11 wherein the light detector further comprises at least one of an amplifier of an output signal of the light detector, an analog band-path filter of the digital pilot signal, and an analog-to-digital converter of an output signal of the analog band-path filter.

13. The apparatus of claim 11 wherein the digital signal processor comprises a series network including:

a digital correlation filter recovering at least on of the digital pilot signal and a first harmonic of the digital pilot signal; and

a digital synchronous demodulator of the recovered digital pilot signal.

14. The apparatus of claim 11 wherein the digital pilot signal is a digitized sinusoidal signal having a frequency in range from about 1 to 2 kHz.

15. The apparatus of claim 13 wherein a ratio of a sampling rate of the digital correlation filter to the frequency of the digital pilot signal is about 10 to 20.

16. The apparatus of claim 13 wherein a data sampling period of the correlation filter comprises at least 8 periods of the digital pilot signal.

17. An apparatus for controlling a bias voltage of an input Mach-Zender modulator (MZM) and an output MZM coupled for performing a return-to-zero (RZ) modulation or a carrier suppressed RZ (CSRZ) modulation of an optical signal, comprising:

a generator of a digital pilot signal for modulating the input MZM and the output MZM;

a first bias circuit of the input MZM;

a second bias circuit of the output MZM;

a light detector of a portion of an optical output signal from the output MZM;

a digital signal processor processing an output signal of the light detector; and

a time multiplexing circuit comprising a timing circuit controlling a first multiplexer and a second multiplexer,

wherein the first multiplexer couples the digital pilot signal to the input MZM or the output MZM and the second multiplexer couples an output of the digital signal processor to a control input of the bias circuit of the MZM concurrently coupled to the digital pilot signal.

18. The apparatus of claim 17 wherein the light detector further comprises at least one of an amplifier of an output signal of the light detector, an analog band-path filter of the digital pilot signal, and an analog-to-digital converter of an output signal of the analog band-path filter.

19. The apparatus of claim 18 wherein the digital signal processor comprises a series network including:

a digital correlation filter recovering at least on of the digital pilot signal and a first harmonic of the digital pilot signal; and

a digital synchronous demodulator of the recovered digital pilot signal.

20. The apparatus of claim 17 wherein the digital pilot signal is a digitized sinusoidal signal having a frequency in range from about 1 to 2 kHz.

21. The apparatus of claim 19 wherein a ratio of a sampling rate of the digital correlation filter to the frequency of the digital pilot signal is about 10 to 20.

22. The apparatus of claim 19 wherein a data sampling period of the correlation filter comprises at least 8 periods of the digital pilot signal.